CMOS SyncFIFO™
64 x 9, 256 x 9, 512 x 9, 1,024 x 9, 2,048 x 9, 4,096 x 9 and 8,192 x 9

IDT72421, IDT72201
IDT72211, IDT72221
IDT72231, IDT72241
IDT72251

FEATURES:

- **64 x 9-bit organization (IDT72421)**
- **256 x 9-bit organization (IDT72201)**
- **512 x 9-bit organization (IDT72211)**
- **1,024 x 9-bit organization (IDT72221)**
- **2,048 x 9-bit organization (IDT72231)**
- **4,096 x 9-bit organization (IDT72241)**
- **8,192 x 9-bit organization (IDT72251)**
- **10 ns read/write cycle time**
- **Read and Write Clocks can be independent**
- **Dual-Ported zero fall-through time architecture**
- **Empty and Full Flags signal FIFO status**
- **Programmable Almost-Empty and Almost-Full flags can be set to any depth**
- **Programmable Almost-Empty and Almost-Full flags default to Empty+7, and Full-7, respectively**
- **Output enable puts output data bus in high-impedance state**
- **Advanced submicron CMOS technology**
- **Available in the 32-pin plastic leaded chip carrier (PLCC) and 32-pin Thin Quad Flat Pack (TQFP)**
- **For through-hole product please see the IDT72420/72200/72210/ 72220/72230/72240 data sheet**
- **Industrial temperature range (–40°C to +85°C) is available**
- **Green parts available, see ordering information**
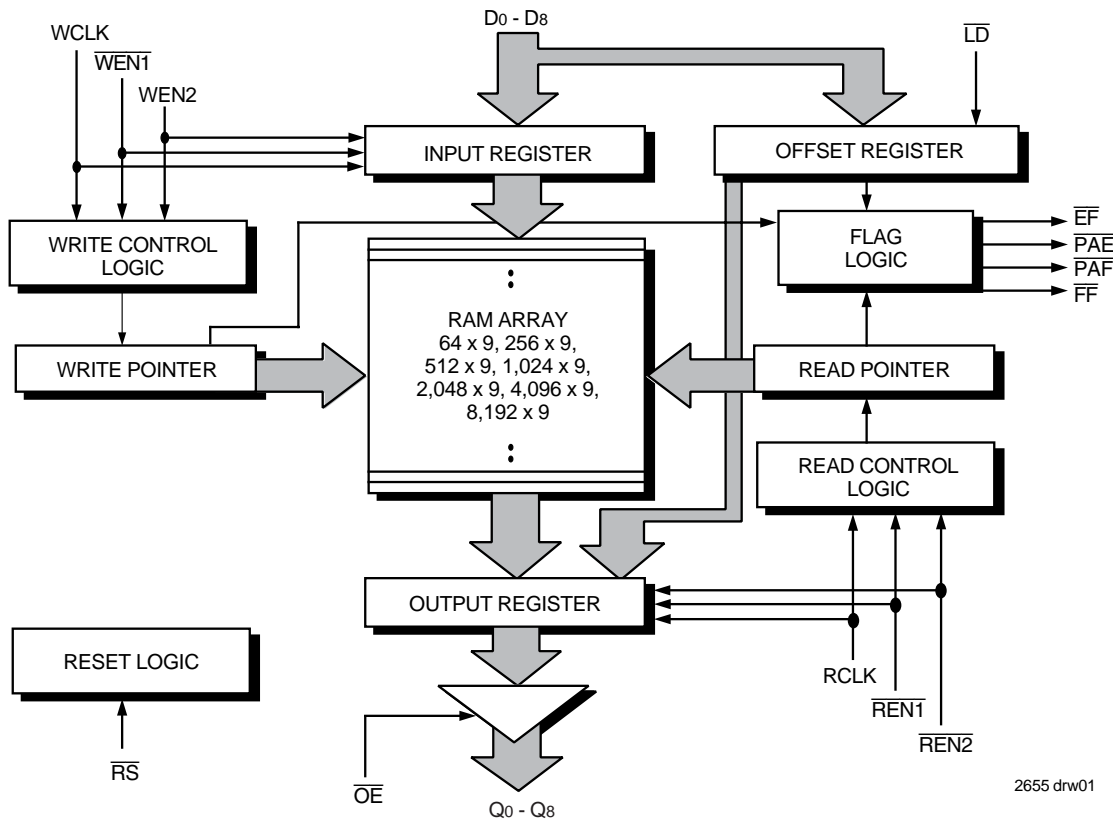
DESCRIPTION:

The IDT72421/72201/72211/72221/72231/72241/72251 SyncFIFO™ are very high-speed, low-power First-In, First-Out (FIFO) memories with clocked read and write controls. These devices have a 64, 256, 512, 1,024, 2,048, 4,096, and 8,192 x 9-bit memory array, respectively. These FIFOs are applicable for a wide variety of data buffering needs such as graphics, local area networks and interprocessor communication.

These FIFOs have 9-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and two write enable pins ($\overline{WEN1}$, WEN2). Data is written into the Synchronous FIFO on every rising clock edge when the write enable pins are asserted. The output port is controlled by another clock pin (RCLK) and two read enable pins ($\overline{REN1}$, $\overline{REN2}$). The Read Clock can be tied to the Write Clock for single clock operation or the two clocks can run asynchronous of one another for dual-clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

The Synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$). Two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$), are provided for improved system control. The programmable flags default to Empty+7 and Full-7 for $\overline{PAE}$ and $\overline{PAF}$, respectively. The programmable flag offset loading is controlled by a simple state machine and is initiated by asserting the load pin ($\overline{LD}$).

These FIFOs are fabricated using IDT's high-speed submicron CMOS technology.

FUNCTIONAL BLOCK DIAGRAM

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COMMERCIAL AND INDUSTRIAL TEMPERATURE RANGES

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IDT72421/72201/72211/72221/72231/72241/72251 CMOS SyncFIFO™
64 x 9, 256 x 9, 512 x 9, 1,024 x 9, 2,048 x 9, 4,096 x 9 and 8,192 x 9

COMMERCIAL AND INDUSTRIAL
TEMPERATURE RANGES

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Com'l & Ind'l	Unit
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T_{STG}	Storage Temperature	−55 to +125	°C
I_{OUT}	DC Output Current	−50 to +50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Commercial/Industrial	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial/Industrial	2.0	—	—	V
V_{IL}	Input Low Voltage Commercial/Industrial	—	—	0.8	V
T_A	Operating Temperature Commercial	0	—	+70	°C
T_A	Operating Temperature Industrial	−40	—	+85	°C

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Industrial: V_{CC} = 5V ± 10%, T_A = −40°C to +85°C)

Symbol	Parameter	IDT72421 IDT72201 IDT72211 IDT72221 IDT72231 IDT72241 Com'l and Ind'l[1] t_{CLK} = 10, 15, 25 ns			IDT72251 Com'l and Ind'l[1] t_{CLK} = 10, 15, 25 ns		
		Min.	Typ.	Max.	Min.	Typ.	Max.
I_{LI}[2]	Input Leakage Current (Any Input)	−1	—	1	−1	—	1
I_{LO}[3]	Output Leakage Current	−10	—	10	−10	—	10
V_{OH}	Output Logic "1" Voltage, I_{OH} = −2mA	2.4	—	—	2.4	—	—
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8mA	—	—	0.4	—	—	0.4
I_{CC1}[4,5,6]	Active Power Supply Current	—	—	35	—	—	50
I_{CC2}[4,7]	Standby Current	—	—	5	—	—	5

NOTES:

1. Industrial temperature range product for the 15ns and 25ns speed grades are available as standard product.
2. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
3. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
4. Tested with outputs open (I_{OUT} = 0).
5. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.
6. Typical I_{CC1} = 1.7 + 0.7*fs + 0.02*C_L*fs (in mA).
   These equations are valid under the following conditions:
   V_{CC} = 5V, T_A = 25°C, fs = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fs/2, C_L = capacitive load (in pF).
7. All Inputs = V_{CC} - 0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20 MHz.

IDT72421/72201/72211/72221/72231/72241/72251 CMOS SyncFIFO™
64 x 9, 256 x 9, 512 x 9, 1,024 x 9, 2,048 x 9, 4,096 x 9 and 8,192 x 9

COMMERCIAL AND INDUSTRIAL
TEMPERATURE RANGES

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Industrial: V_{CC} = 5V ± 10%, T_A = −40°C to +85°C)

Symbol	Parameter	Commercial IDT72421L10 IDT72201L10 IDT72211L10 IDT72221L10 IDT72231L10 IDT72241L10 IDT72251L10 Min.	Max.	Com'l & Ind'l[1] IDT72421L15 IDT72201L15 IDT72211L15 IDT72221L15 IDT72231L15 IDT72241L15 IDT72251L15 Min.	Max.	Com'l & Ind'l[1] IDT72421L25 IDT72201L25 IDT72211L25 IDT72221L25 IDT72231L25 IDT72241L25 IDT72251L25 Min.	Max.	Unit
f_S	Clock Cycle Frequency	—	100	—	66.7	—	40	MHz
t_A	Data Access Time	2	6.5	2	10	2	15	ns
t_{CLK}	Clock Cycle Time	10	—	15	—	25	—	ns
t_{CLKH}	Clock High Time	4.5	—	6	—	10	—	ns
t_{CLKL}	Clock Low Time	4.5	—	6	—	10	—	ns
t_{DS}	Data Setup Time	3	—	4	—	6	—	ns
t_{DH}	Data Hold Time	0.5	—	1	—	1	—	ns
t_{ENS}	Enable Setup Time	3	—	4	—	6	—	ns
t_{ENH}	Enable Hold Time	0.5	—	1	—	1	—	ns
t_{RS}	Reset Pulse Width[2]	10	—	15	—	15	—	ns
t_{RSS}	Reset Setup Time	8	—	10	—	15	—	ns
t_{RSR}	Reset Recovery Time	8	—	10	—	15	—	ns
t_{RSF}	Reset to Flag and Output Time	—	10	—	15	—	25	ns
t_{OLZ}	Output Enable to Output in Low-Z[3]	0	—	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid	3	6	3	8	3	13	ns
t_{OHZ}	Output Enable to Output in High-Z[3]	3	6	3	8	3	13	ns
t_{WFF}	Write Clock to Full Flag	—	6.5	—	10	—	15	ns
t_{REF}	Read Clock to Empty Flag	—	6.5	—	10	—	15	ns
t_{PAF}	Write Clock to Programmable Almost-Full Flag	—	6.5	—	10	—	15	ns
t_{PAE}	Read Clock to Programmable Almost-Empty Flag	—	6.5	—	10	—	15	ns
t_{SKEW1}	Skew time between Read Clock & Write Clock for Empty Flag & Full Flag	5	—	6	—	10	—	ns
t_{SKEW2}	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Programmable Almost-Full Flag	14	—	15	—	18	—	ns

NOTES:
1. Industrial temperature range product for the 15ns and 25ns speed grades are available as standard product.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE (T_a = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}[2]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:
1. With output deselected (OE ≥ V_{IH}).
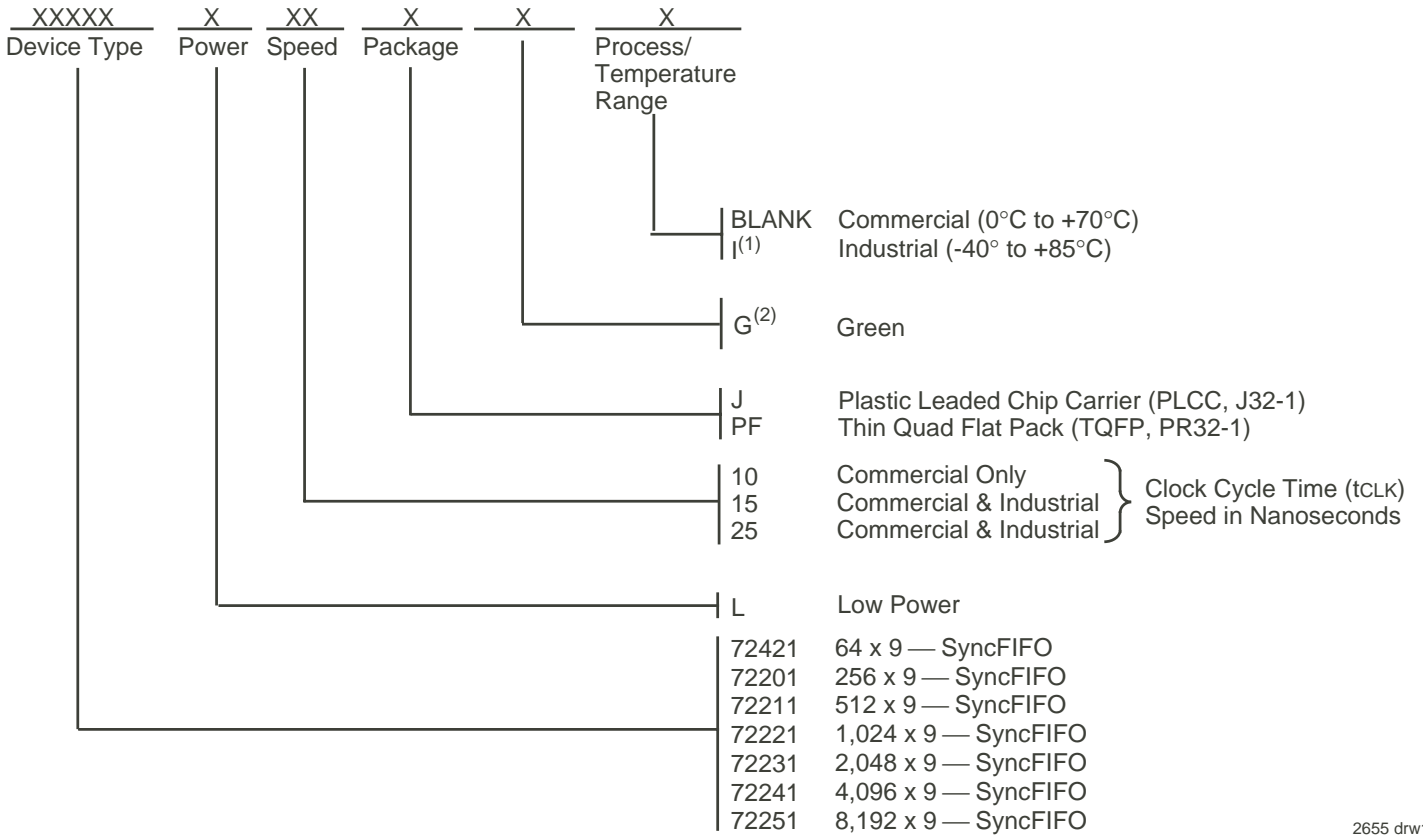2. Characterized values, not currently tested.

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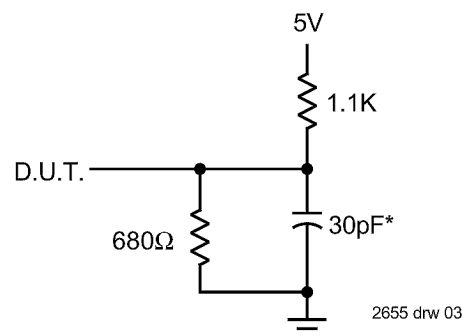
or equivalent circuit

Figure 1. Output Load
*includes jig and scope capacitances

ORDERING INFORMATION

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 XXXXX        X     XX      X       X         X
Device Type  Power Speed  Package          Process/
                                           Temperature
                                           Range
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BLANK	Commercial (0°C to +70°C)
I[1]	Industrial (-40° to +85°C)

G[2]	Green

J	Plastic Leaded Chip Carrier (PLCC, J32-1)
PF	Thin Quad Flat Pack (TQFP, PR32-1)

10	Commercial Only	Clock Cycle Time (t_{CLK})
15	Commercial & Industrial	Speed in Nanoseconds
25	Commercial & Industrial	

L	Low Power

72421	64 x 9 — SyncFIFO
72201	256 x 9 — SyncFIFO
72211	512 x 9 — SyncFIFO
72221	1,024 x 9 — SyncFIFO
72231	2,048 x 9 — SyncFIFO
72241	4,096 x 9 — SyncFIFO
72251	8,192 x 9 — SyncFIFO

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NOTES:
1. Industrial temperature range product for the 15ns and 25ns speed grades are available as standard product.
2. Green parts are available. For specific speeds and packages contact your sales office.